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l7 and l6	1

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 result set
*DB=USPT; PLUR=YES; OP=ADJ*

<u>L8</u>	l7 and l6	1	<u>L8</u>
<u>L7</u>	data NEAR10 range\$1	42532	<u>L7</u>
<u>L6</u>	l5 and l4	5	<u>L6</u>
<u>L5</u>	369/\$	39082	<u>L5</u>
<u>L4</u>	l3 and l2	6	<u>L4</u>
<u>L3</u>	resync\$ NEAR10 pattern\$1	257	<u>L3</u>
<u>L2</u>	(determin\$ or calculat\$) NEAR10 l1	232	<u>L2</u>
<u>L1</u>	DSV or digital sum value	730	<u>L1</u>

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L8: Entry 1 of 1

File: USPT

Oct 28, 1997

US-PAT-NO: 5682153

DOCUMENT-IDENTIFIER: US 5682153 A

TITLE: Adjust bit determining circuit

DATE-ISSUED: October 28, 1997

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Ishiguro; Masayuki	Kasugai			JPX

US-CL-CURRENT: 341/53; 341/58, 341/59, 360/40